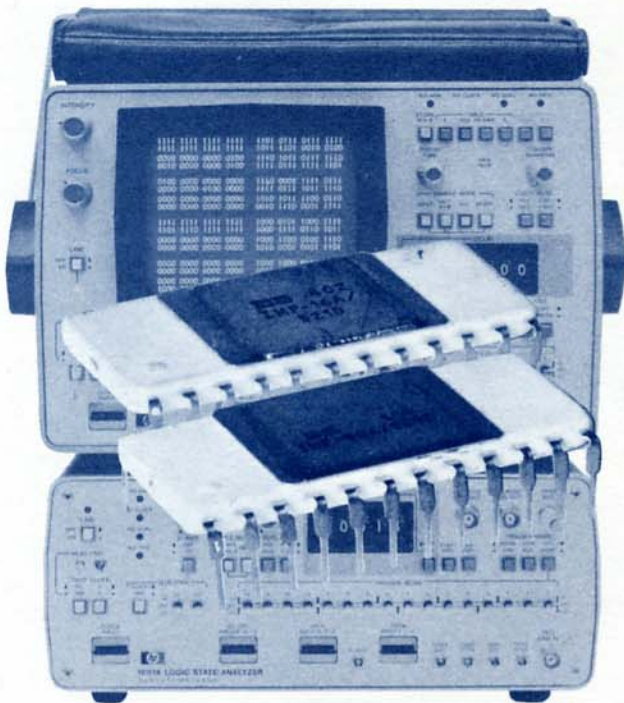


APPLICATION NOTE 167-17
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of National IMP microprocessor systems.



HEWLETT  PACKARD

1. INTRODUCTION.

This application note is intended to assist the user of National Semiconductor Corp. IMP microprocessor devices in the real-time analysis of his system in both design and troubleshooting environments. This note demonstrates real-time analysis of program flow, triggering on a specific event, and use of the paging technique.

The Central Processing Unit (CPU) of the IMP system is configured around the Control Read Only Memory (CROM) device and one (or more) Register and Arithmetic Logic Unit (RALU) device(s) as shown in figure 1.

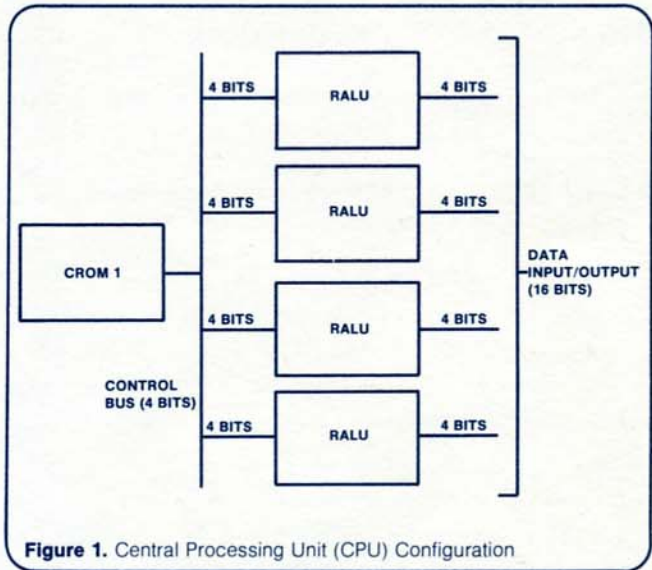
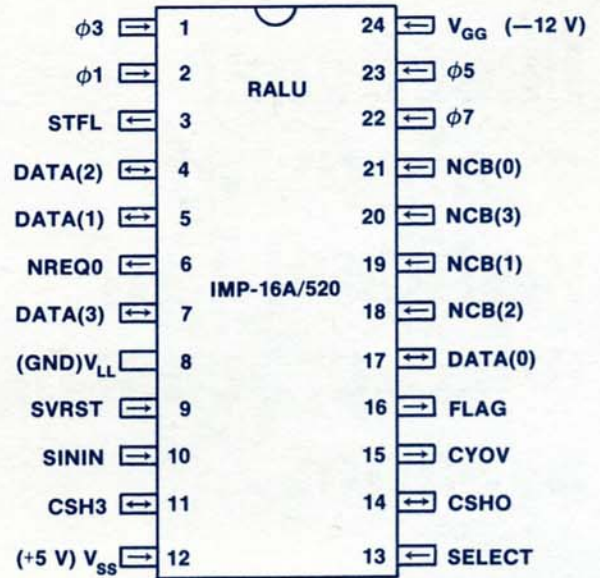
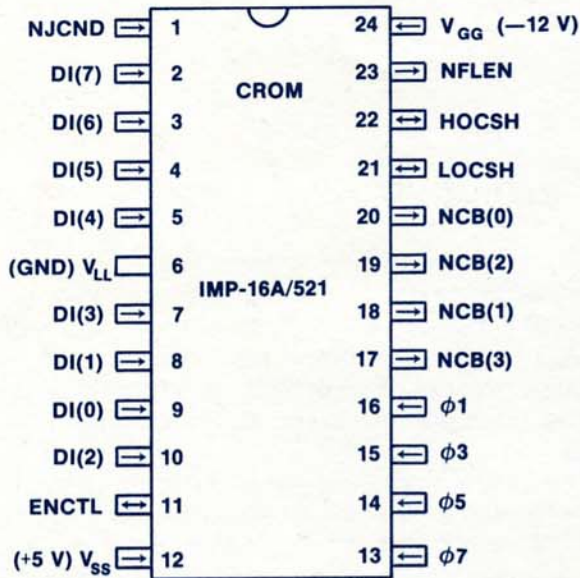


Figure 1. Central Processing Unit (CPU) Configuration

A CROM provides storage for 100 microinstructions of 23-bits each, program sequencing, subroutine execution, and translation of microinstructions into RALU commands. Each RALU provides 96-bits of storage: 4-bits in each of 7 general registers; a status register; and a 16-word last-in/first-out (LIFO) stack. The RALU also contains provisions for: an arithmetic/logic unit to perform ADD, AND, OR, exclusive OR operations; a shift register; an input/output (I/O) data multiplexer to an external data bus; and a 4-bit, time-multiplexed command bus for RALU control.

Both CROM and RALU chips are constructed using standard P-channel, enhancement mode, silicon gate technology and operate on +5 V and -12 V power supplies with 4-phase, non-overlapping clock signals. Signals interfacing CROM and RALU chips are MOS logic level, while signals interfacing the rest of the system are TTL logic level.

2. PIN ASSIGNMENTS.



PIN NO.

FUNCTION

- 1** Jump condition input from external jump condition multiplexer.
- 2-5 & 7-10** Data input lines carry instructions to CROM instruction register.
- 11** Enable control provides logic "1" when branch to instruction fetch routine occurs. Responds to logic "1" input by executing branch to instruction fetch routine.
- 12** +5 V input.
- 13-16** 4-phase, non-overlapping clock signals.
- 17-20** Command bits to RALU.
- 21** Low-order carry/shift to and from RALU.
- 22** High-order carry/shift to and from RALU.
- 23** Flag enable control output used to set/reset flags addressed by data inputs.
- 24** -12 V input.

PIN NO.

FUNCTION

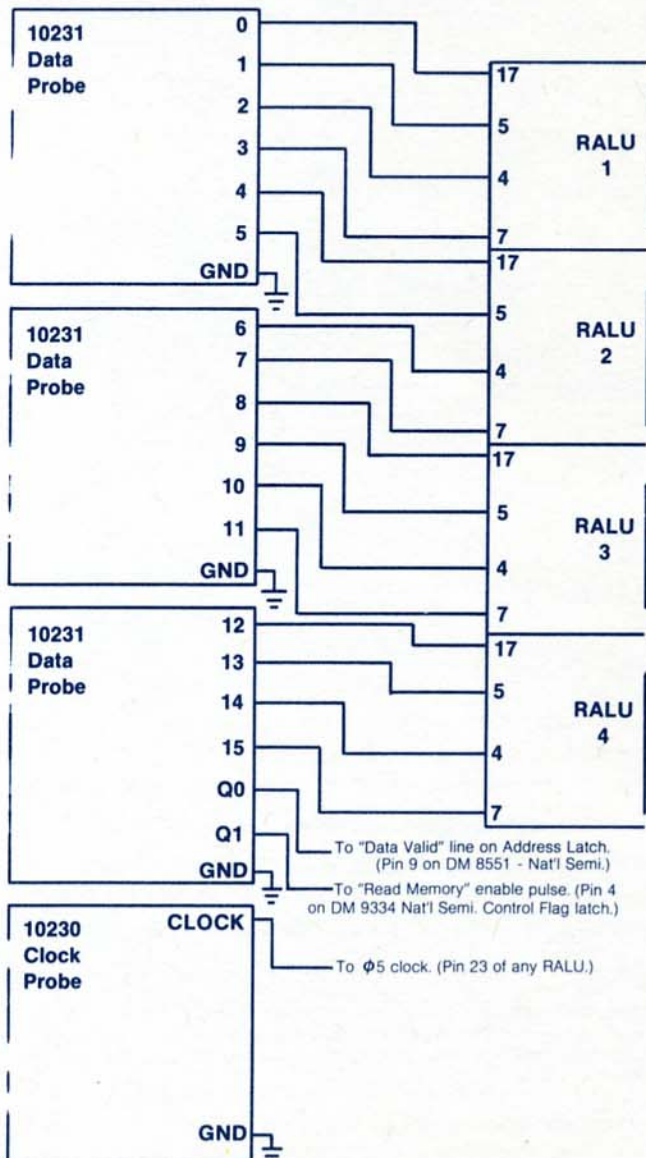
- 1, 2, 22, 23** 4-phase, non-overlapping clock signals.
- 3** Stack full output goes true when bottom word of stack is non-zero at start of previous cycle.
- 4, 5, 7, 17** Transfers data between RALU and memory or peripheral devices.
- 6** Result bus equals zero. Logic level goes to "0" level when R-bus contains all zeroes.
- 9** Save/Restore line. Provides a means of modifying status flags over the data bus.
- 10** SININ accomplishes sign extension.
- 11, 14** Carry input (CSH0) and carry output (CSH3) used primarily for transfer of carry and shift information between RALU's or between RALU and CROM.
- 13** Select flag input used to select carry or overflow and to determine whether the Link is included in shift operations.
- 15** Carry/Overflow provides output signal indicating state of Carry flag or Overflow flag as selected by the select input.
- 16** Flag output indicates state of the general purpose status flag.
- 18-21** Command inputs to RALU.

3. PROBE CONNECTIONS.

All information on address and data acquisition presented in this application note was gathered using the National Semiconductor Corp IMP 16C (Integrated Microprocessor) system. However, the procedures outlined here will be valid for your microprocessor system provided it is configured to meet the requirements for using a single CROM (IMP-16A/521) chip and four RALU (IMP-16A/520) chips, with the appropriate auxiliary circuits and instruction set.

A system that will not "come up" can frequently be debugged by monitoring address flow alone. Since address data in the IMP system is time-multiplexed with data, the address must be latched by external devices such as National Semiconductor part DM 8551. Therefore, the best place to secure address information is at the memory address control lines of the RALU's. The 1600A data probes connected as follows will provide a display of the activity on the address lines.

4. PIN CONNECTIONS.



5. SETTING THE CONTROLS.

Turn power on and set Logic State Analyzer controls as follows:

Display Mode	Table A
Sample Mode ¹	REPET
Trigger Mode	
NORM/ARM	NORM
LOCAL/BUS	LOCAL
OFF/WORD	WORD
Start Display	ON
Clock	⌋
Threshold ²	TTL
All Other Pushbuttons	Out Position
Display Time	ccw
Column Blanking	ccw
Qualifier	
Q0	LO
Q1	HI
Trigger Word	
Switches	set to Address at which you wish to trigger

¹ If program is not looping or cycling through the selected address, select SGL, press RESET, and start your system. The first time the system passes through the trigger point, the display will be generated and stored.

² Should you desire to trigger on a signal line that interfaces CROM with RALU, it may be necessary to switch to VAR and adjust to proper MOS level.

6. DISPLAY INTERPRETATION.

When power is first applied to the microprocessor system, all RALU registers, flags, and the stack are cleared to zero. In this illustration, system response to a program for clearing all Accumulators to zero is considered. Proper operation is confirmed by a comparison between real-time state analysis, figure 2a, and the assembler listing output, figure 2b.

In this illustration, we trigger on the first address in the actual program sequence, 0079, and display each subsequent address. Note that at address 007C, the operation code includes a subtract instruction affecting Accumulator 1. Line 5 of the table display verifies that the loop to address 0078 does indeed take place, and the instruction is being performed. At the conclusion of the subtract operation, we would expect the system to re-enter the program at address 007D. Line 6 of the table display verifies system operation by displaying address 007D as expected. In a similar manner, each instruction in the routine may be shown to have been properly executed.

To view addresses following the last displayed address, simply set the Trigger Word switches to match the address displayed in line 16. This address then becomes the trigger word in line 1 with the next 15 addresses displayed on lines 2 through 16. If you wish to retain the original trigger point, an alternate technique is to use digital delay and set the thumbwheels to 00015 which provides the same display.

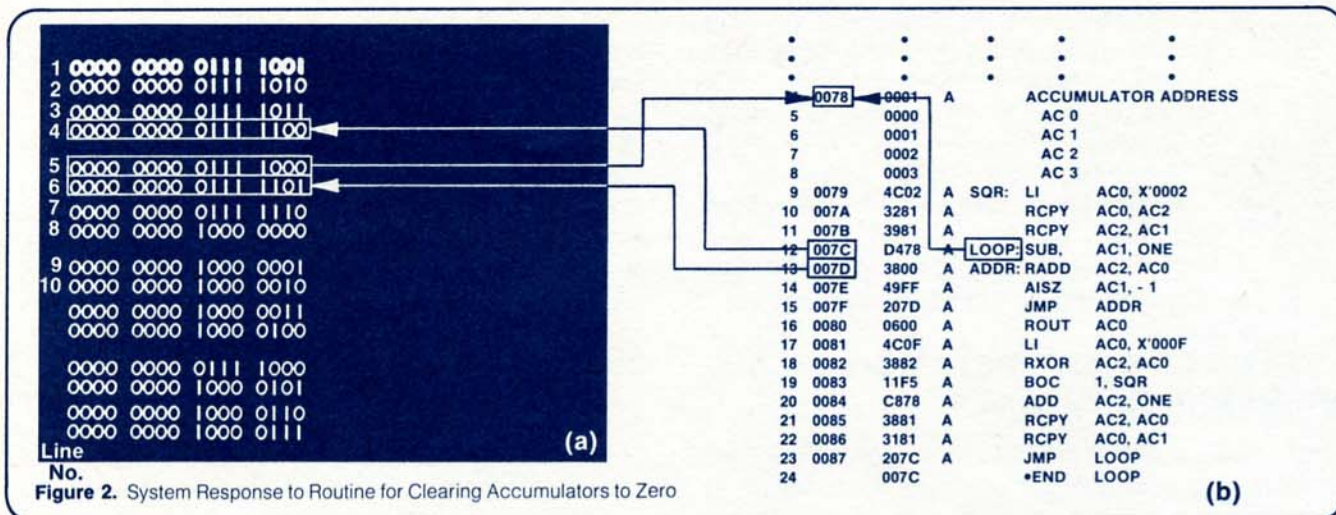


Figure 2. System Response to Routine for Clearing Accumulators to Zero

7. THE MAP.

If a tabular display is not achieved in Sections 5 and 6, it means the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program, switch to MAP NORM. Using the Trigger Word switches, move the cursor to encircle one of the dots as shown in figure 3. Switch to MAP EXP and make final positioning of the cursor. The No Trigger light will now go out and switching back to Table A displays the 16 addresses around that point.

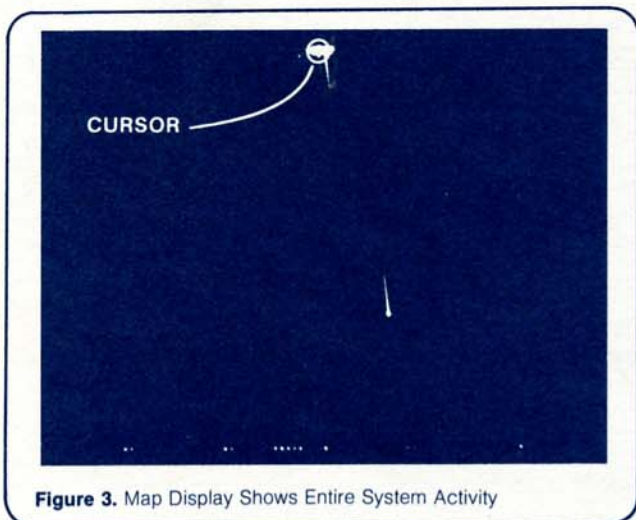


Figure 3. Map Display Shows Entire System Activity

8. VIEWING ADDRESS AND DATA.

When program deviations are found, the reason may be as simple as program error or as complicated as a hardware failure on the Data bus, the Control bus or other command lines. Additional input channels now become very desirable.

By combining the 1600A and 1607A, the display and trigger capability can be expanded to 32-bits

wide allowing 16-bit addresses and 16-bits of data or active command signals to be viewed simultaneously. The hook-up is easy:

1. Connect data cable between rear panel connectors.
2. Connect a cable from PATTERN TRIG OUT on 1600A to TRIG ARM IN on 1607A.
3. Set 1600A controls as detailed in Section 5 with the following exception: set display mode to A & B.
4. Set 1607A controls as follows:

Sample Mode REPET
 Trigger Mode
 NORM/ARM ARM
 LOCAL/BUS LOCAL
 OFF/WORD OFF
 Start Display ON
 Clock
 Qualifier
 DSPLY/TRIG DSPLY
 Q0 HI
 Q1 LO or OFF
 Trigger Word OFF (don't care)
 Threshold same as 1600A
 Display Time ccw
 Column Blanking ccw

5. Connect 1600A data and clock probes as described in Section 4.
6. Connect 1607A data and clock probes as follows:
 - a. Connect 1607A data input lines 0 through 15 in parallel with corresponding 1600A data probe lines.

- b. Connect Q0 to the Read Memory flag signal which appears at the Input Multiplexer (National Semiconductor DM 8123 or equivalent). Leave Q1 probe unconnected.
- c. Connect Clock probe to $\phi 7$ clock at pin 22 of any RALU.
- d. Connect grounds to appropriate point(s).

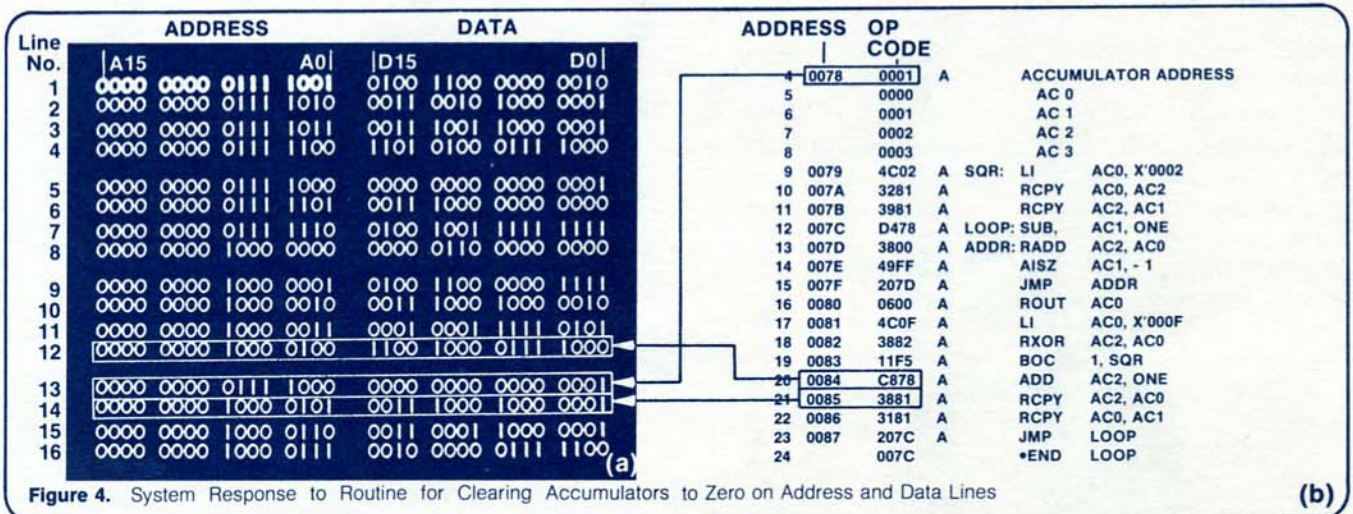
9. DISPLAY INTERPRETATION OF ADDRESS AND DATA LINES.

Let's look again at the sample program, figure 4b. By displaying both address and data, it is possible to confirm exact system operation with respect to the routine for clearing the Accumulators to Zero.

For example, line 12 of the state display, figure 4a, shows an operating code which requires an add operation in Accumulator 2. Line 13 of the state display verifies that the accumulators are indeed addressed so the add instruction may be performed. Upon completion of the add instruction, we would anticipate a return to the next address in the program. That this is indeed accomplished is verified by line 14 of the state display where address 0085 and operating code 3881 are displayed.

In a similar manner, each line of the display can be examined to reveal exact program operation.

To observe the action of other control lines, connect Q1 probe on the 1607A to the desired point in the circuit. Setting Qualifier Q1 switch to the HI or LO position, as required by the selected control line state, it is possible to view the effect of the command line on the display.





Application Notes in the 167 series with the primary instrument(s) used in parenthesis.

- | | |
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| 167-2 Digital Triggering for Analog Measurements (1601L). | 167-13 The Role of Logic State Analyzers in Microprocessor Based Designs (1600A and 1607A). |
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